FIG. 1

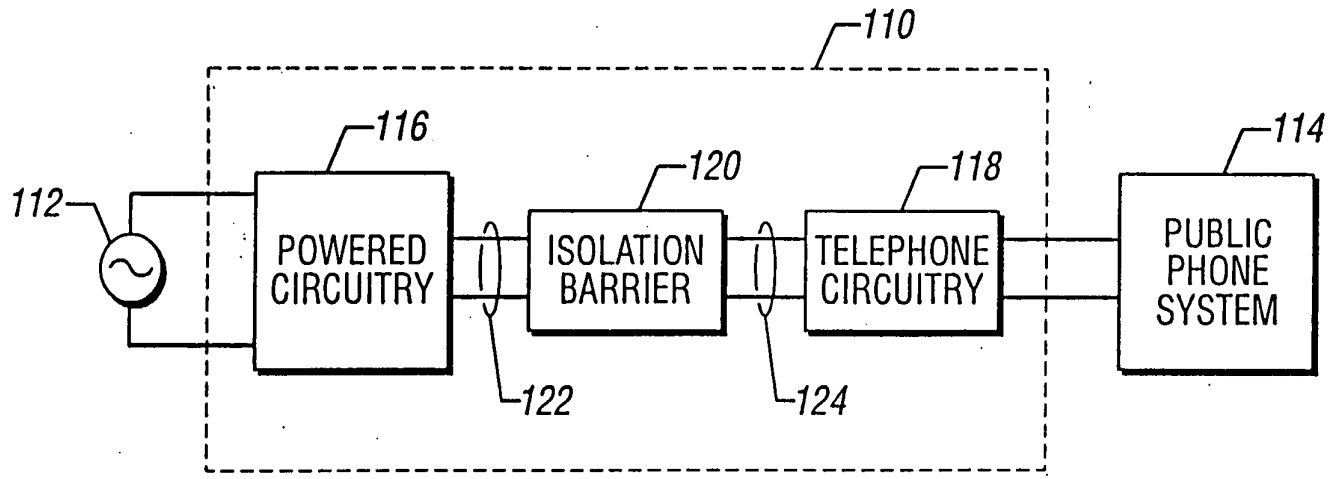


FIG. 2

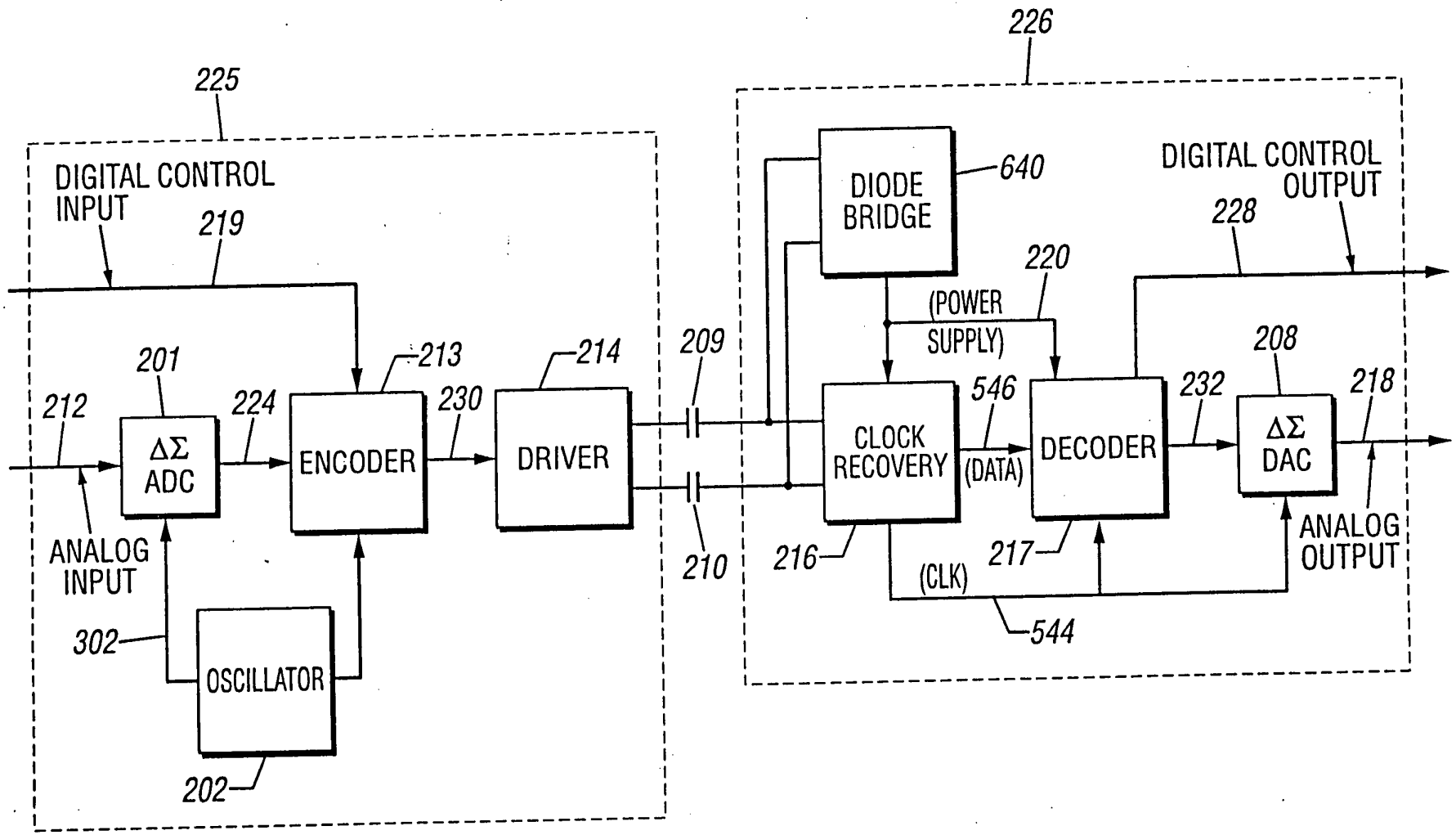

225
DIGITAL CONTROL INPUT
219
201
212
224
213
230
214
209
ANALOG INPUT
ΔΣ ADC
ENCODER
DRIVER
302
OSCILLATOR
202
210
226
DIODE BRIDGE
640
DIGITAL CONTROL OUTPUT
228
220
(POWER SUPPLY)
208
546
232
218
CLOCK RECOVERY
(DATA)
DECODER
ΔΣ DAC
ANALOG OUTPUT
216
217
(CLK)
544

FIG. 3A

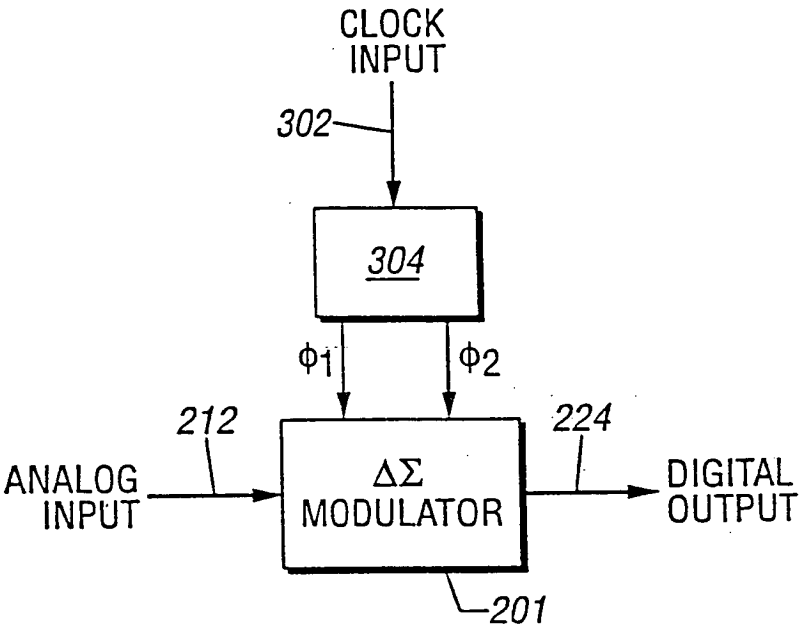

CLOCK INPUT
302
304
Φ1
Φ2
212
224
ANALOG INPUT
ΔΣ MODULATOR
DIGITAL OUTPUT
201

FIG. 3B

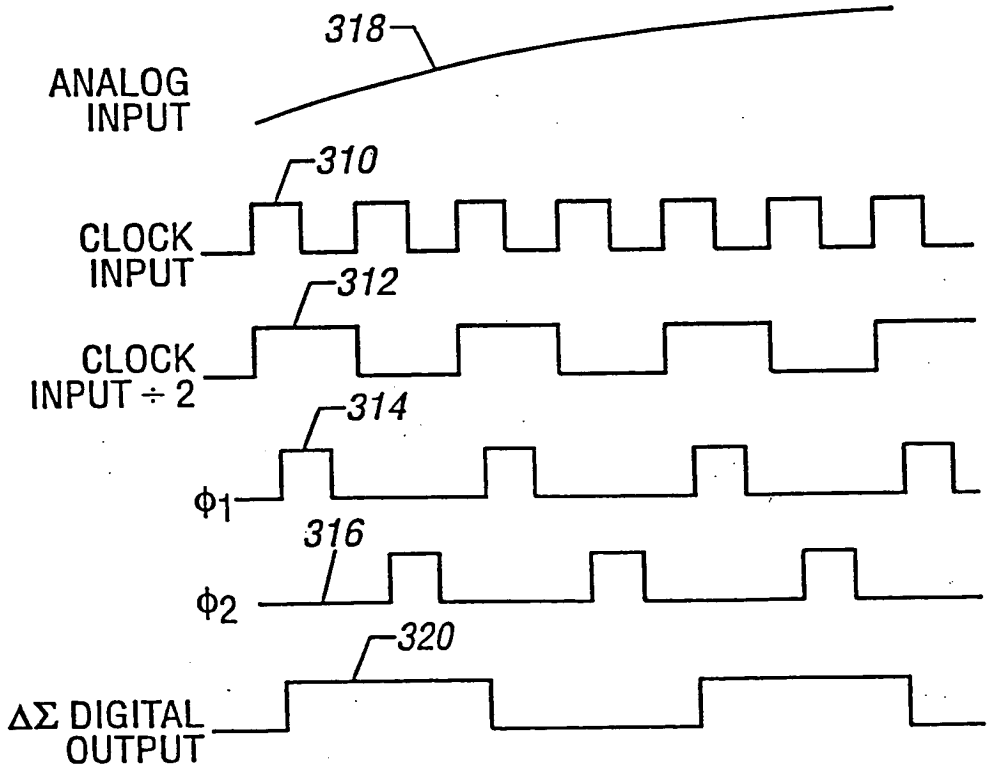

318
ANALOG INPUT
310
CLOCK INPUT
312
CLOCK INPUT ÷ 2
314
Φ1
316
Φ2
320
ΔΣ DIGITAL OUTPUT

FIG. 4A

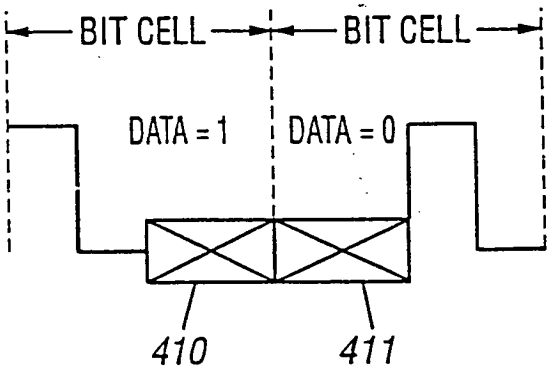


FIG. 4B

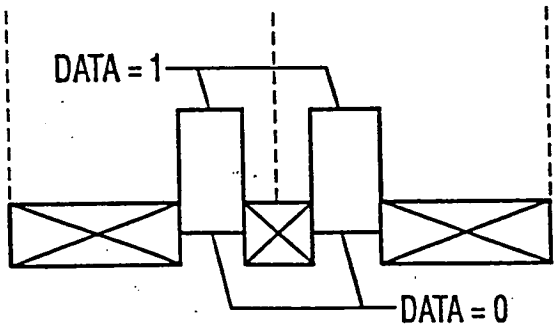


FIG. 5

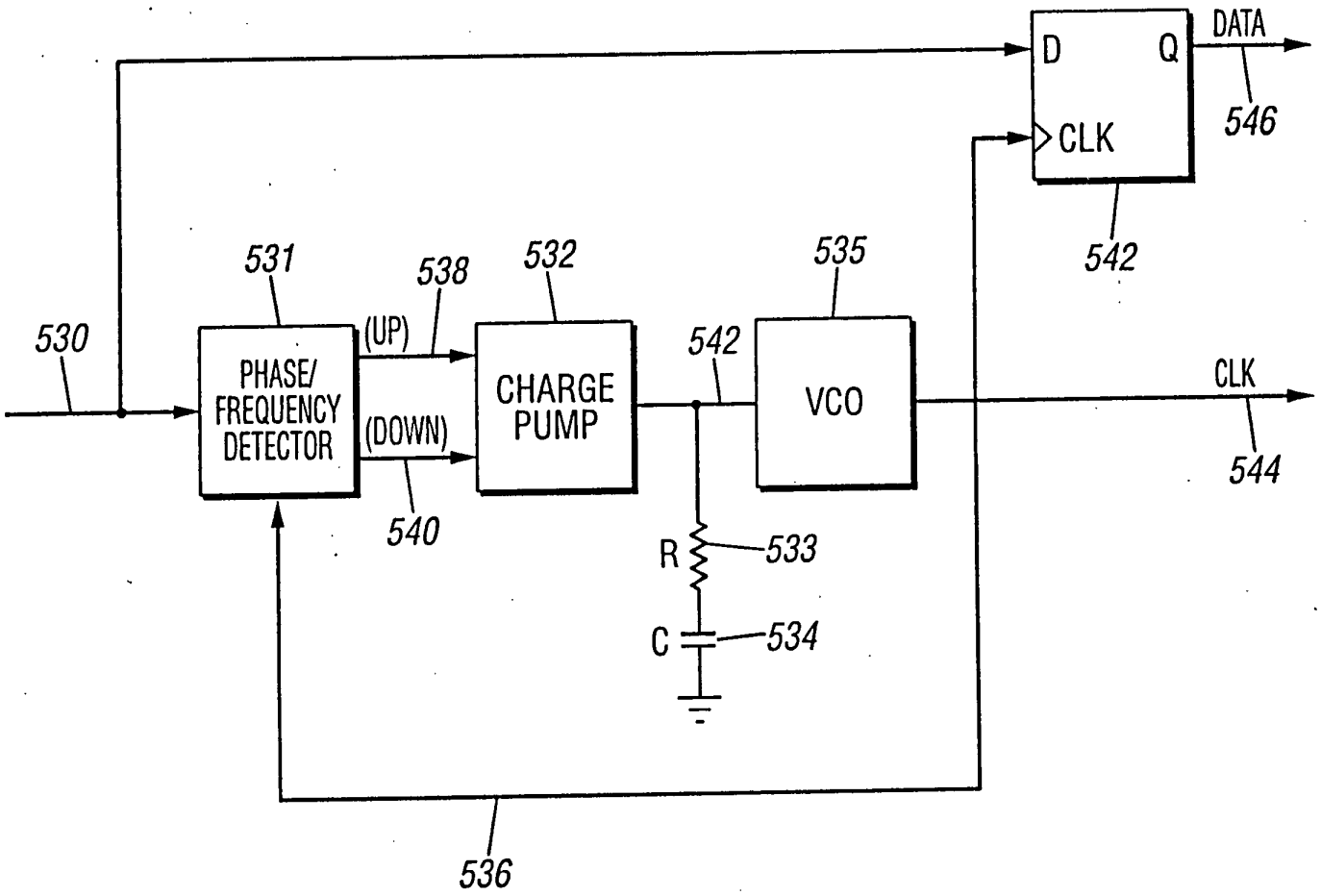

D
Q
DATA
CLK
546
542
531
538
532
535
530
PHASE/
FREQUENCY
DETECTOR
(UP)
(DOWN)
CHARGE
PUMP
542
VCO
CLK
544
540
R
533
C
534
536

FIG. 6A

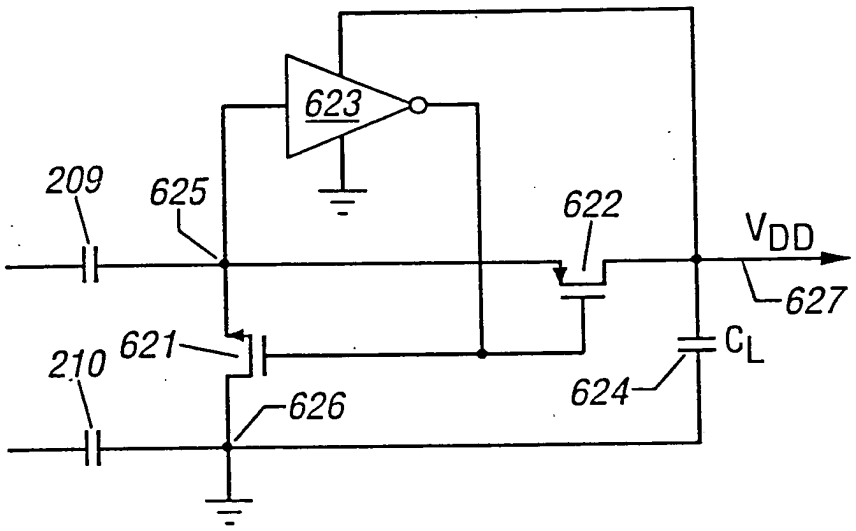
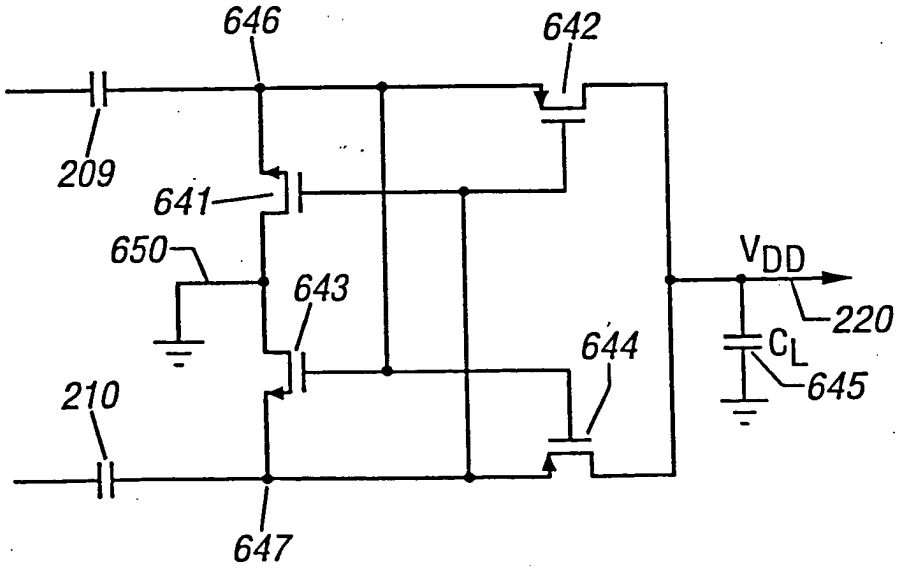

623
209
625
622
V_{DD}
627
621
210
626
624
C_L

FIG. 6B


646
642
209
641
650
643
V_{DD}
220
644
C_L
645
210
647

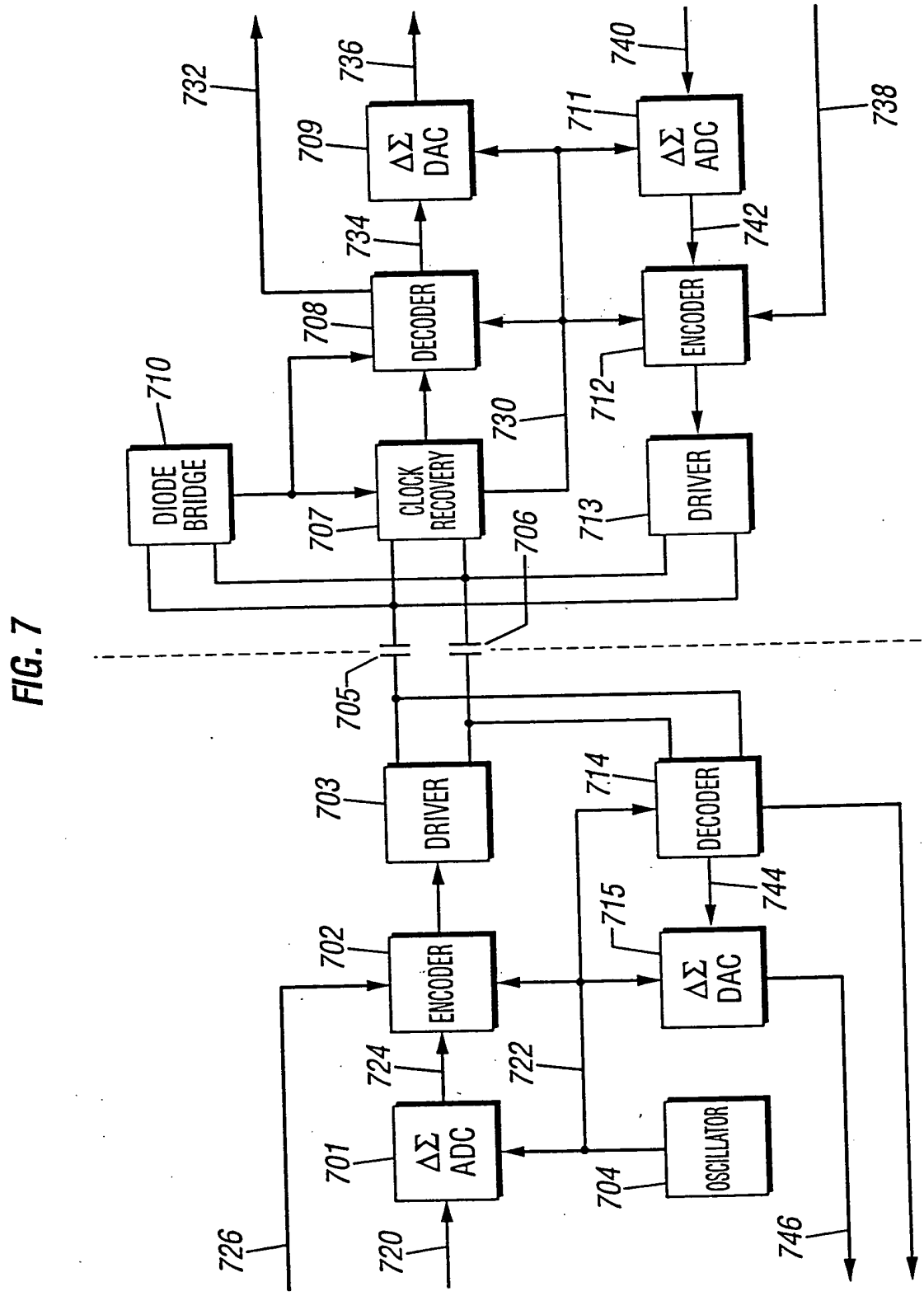

ΔΣ ADC
ENCODER
DRIVER
DECODER
ΔΣ DAC
OSCILLATOR
ΔΣ DAC
ΔΣ ADC
DECODER
ENCODER
DRIVER
CLOCK RECOVERY
DIODE BRIDGE
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
720
722
724
726
730
732
734
736
738
740
742
744
746

FIG. 7

FIG. 8

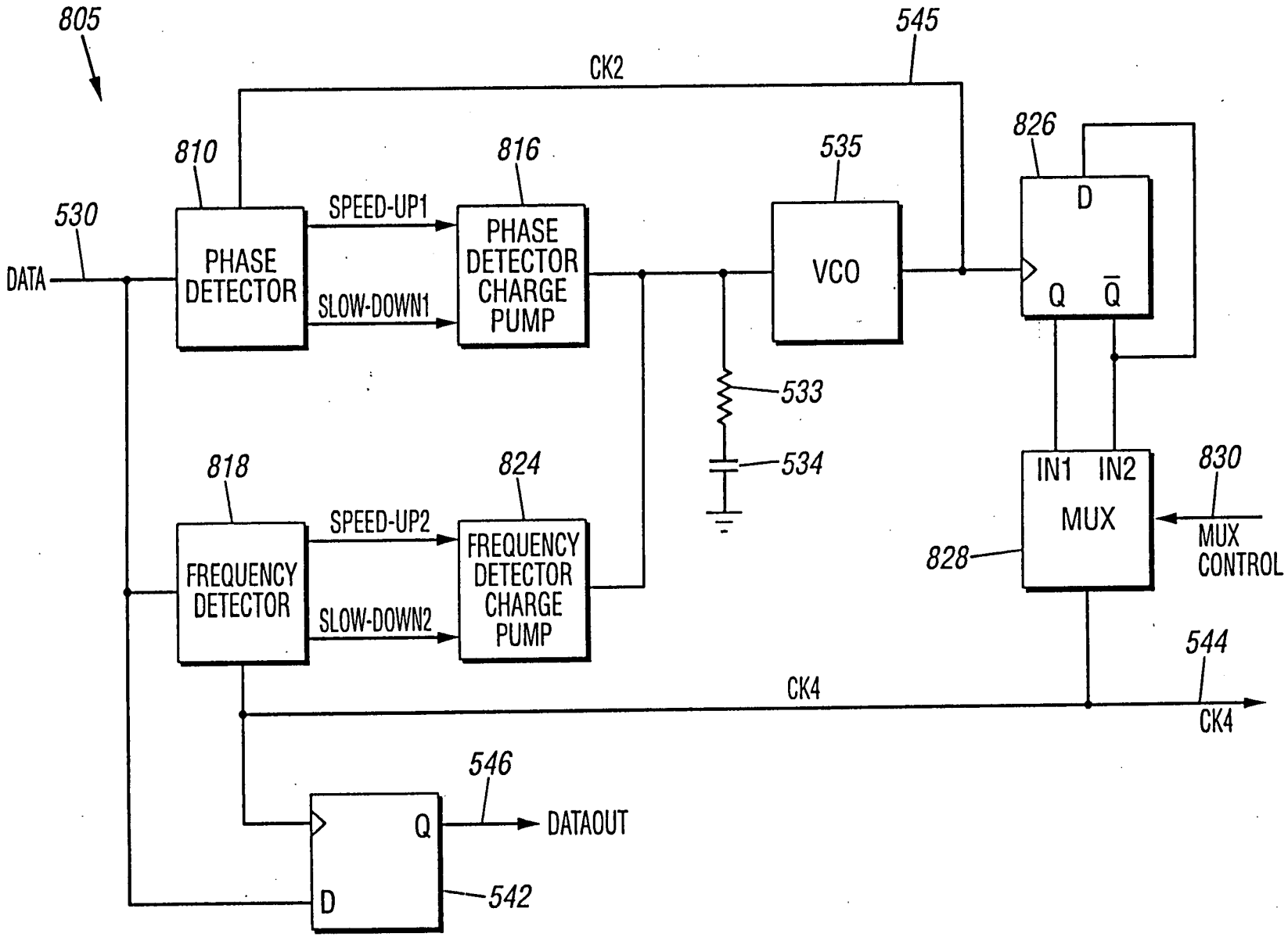

805
545
CK2
826
810
816
535
530
SPEED-UP1
PHASE DETECTOR
PHASE DETECTOR CHARGE PUMP
VCO
D
DATA
SLOW-DOWN1
Q
Q̄
533
534
818
824
830
IN1
IN2
SPEED-UP2
FREQUENCY DETECTOR
FREQUENCY DETECTOR CHARGE PUMP
MUX
MUX CONTROL
828
SLOW-DOWN2
544
CK4
CK4
546
Q
DATAOUT
D
542

FIG. 9

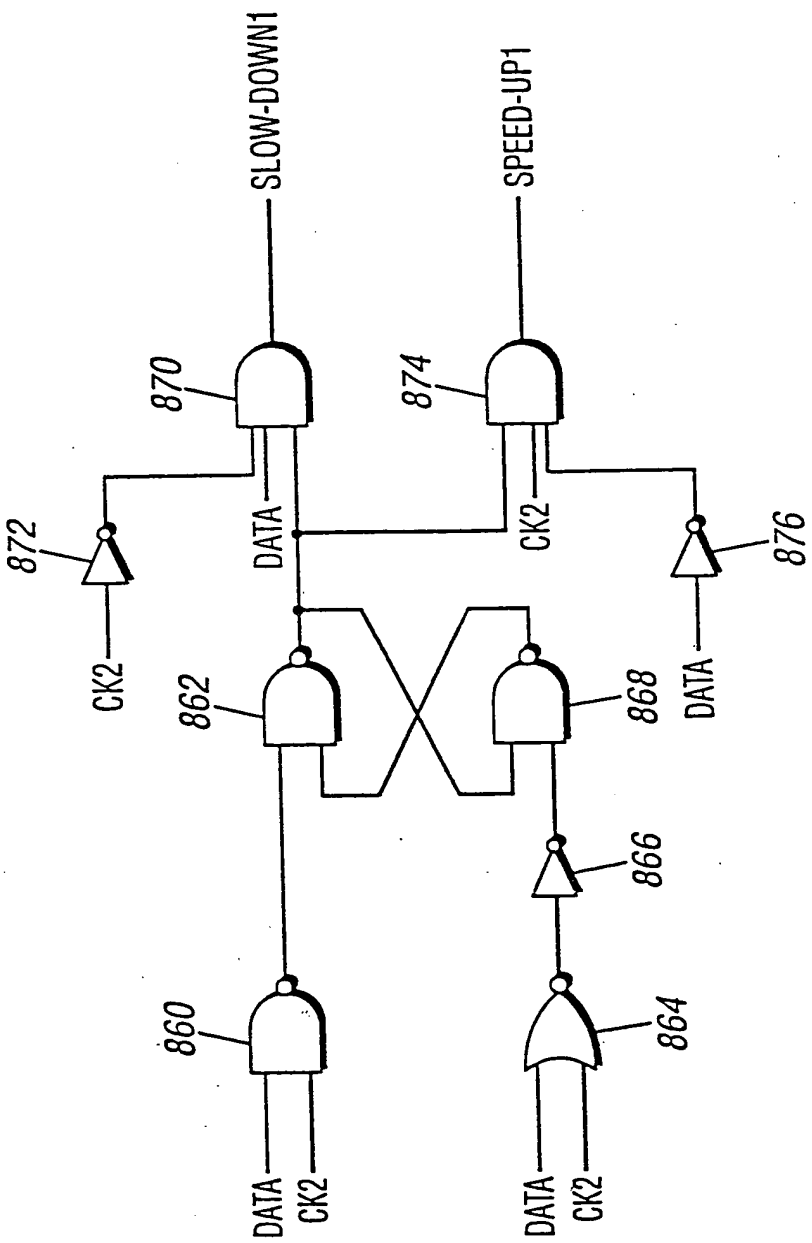

SLOW-DOWN1
SPEED-UP1
870
874
872
876
DATA
CK2
CK2
DATA
862
868
866
860
864
DATA
CK2
DATA
CK2

FIG. 10

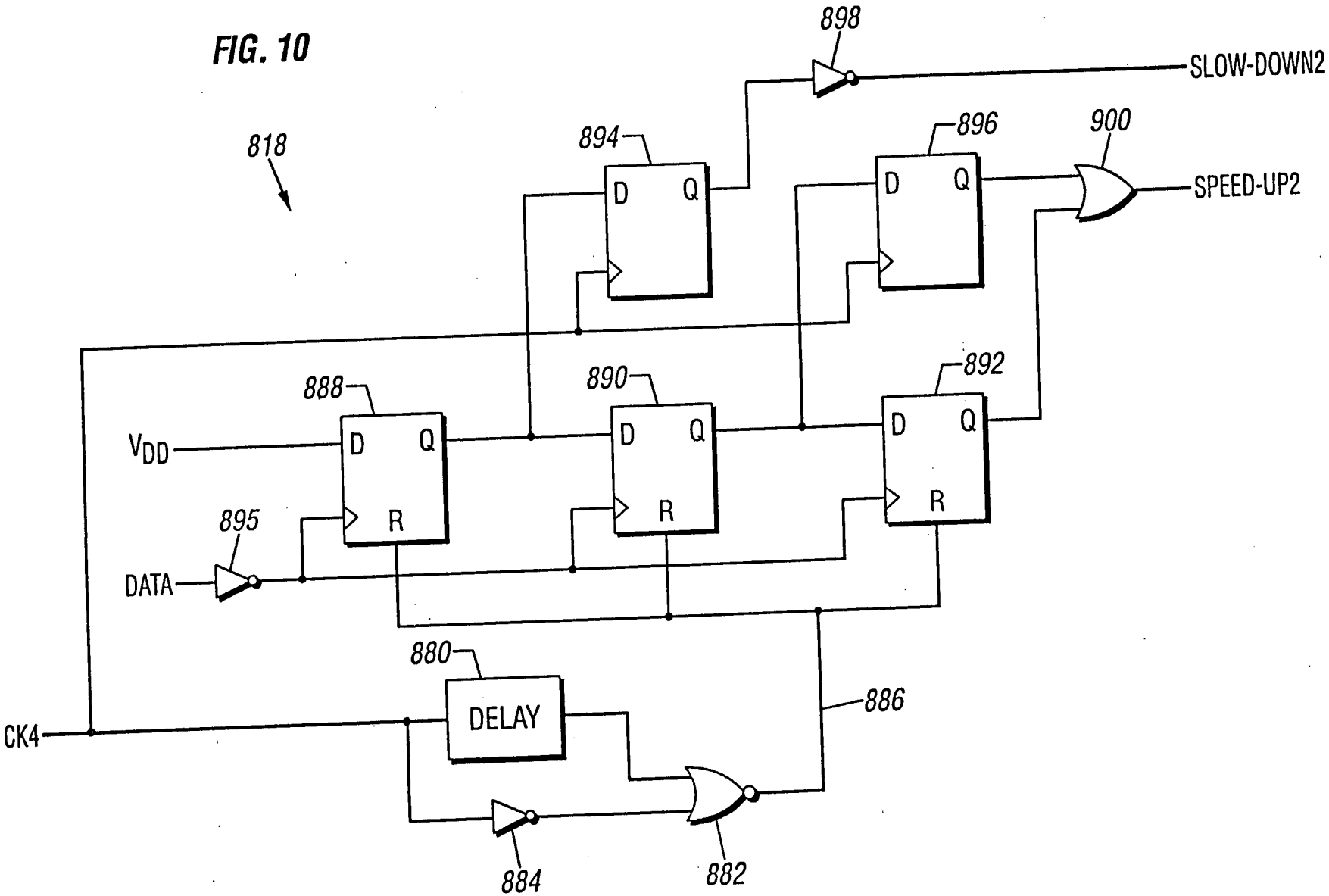

818
898
SLOW-DOWN2
894
896
900
D
Q
SPEED-UP2
888
890
892
V_{DD}
R
895
DATA
880
DELAY
886
CK4
884
882

FIG. 11

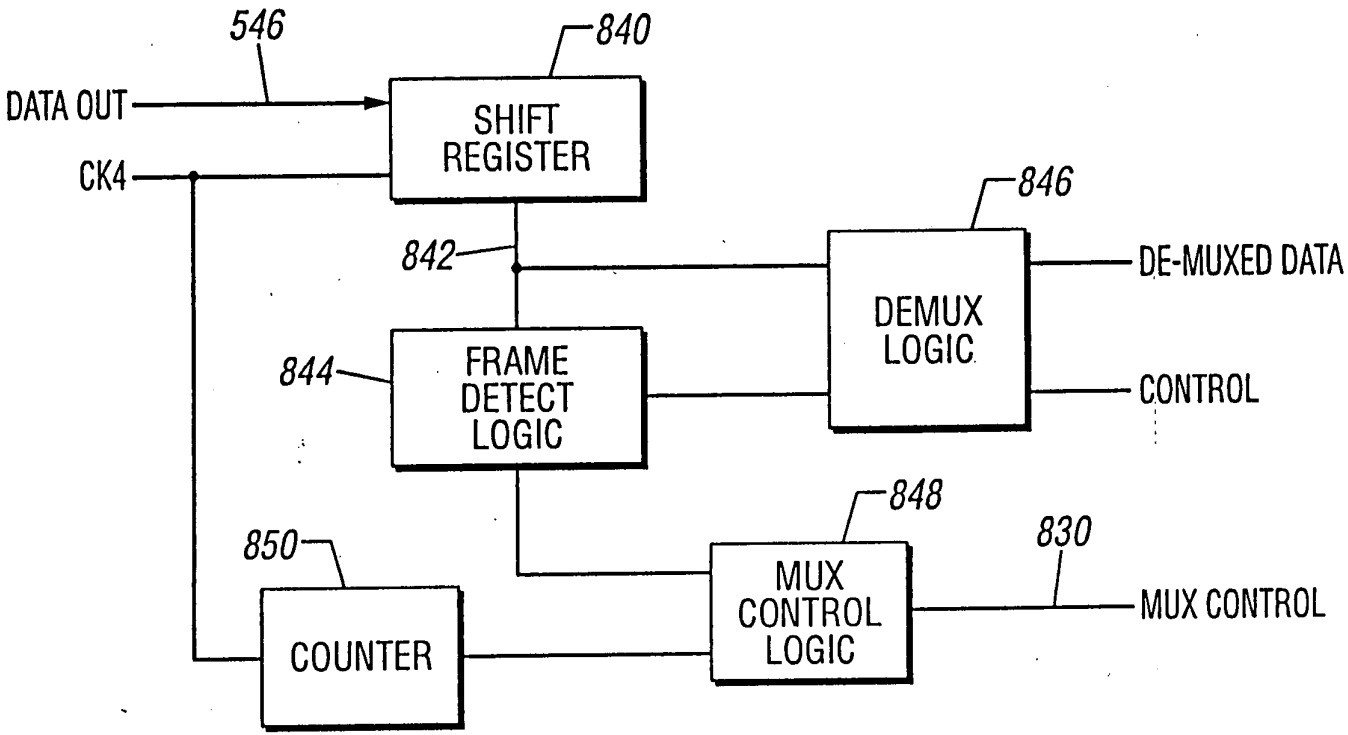

546
840
DATA OUT
SHIFT REGISTER
CK4
846
842
DE-MUXED DATA
DEMUX LOGIC
844
FRAME DETECT LOGIC
CONTROL
848
850
830
MUX CONTROL LOGIC
COUNTER
MUX CONTROL

FIG. 12

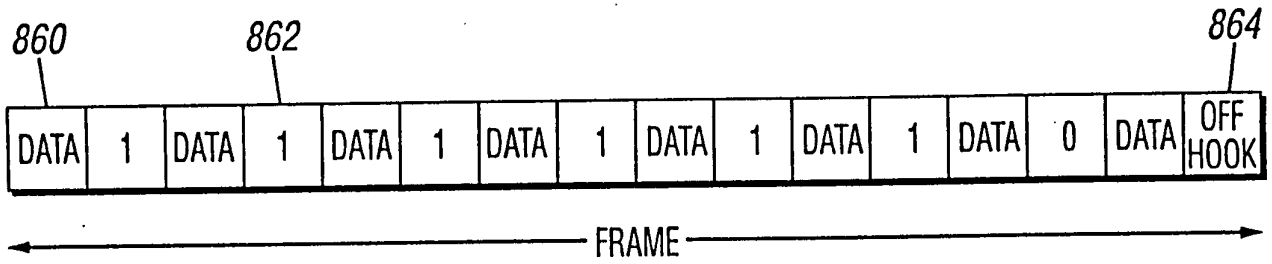

860
862
864
DATA
1
DATA
1
DATA
1
DATA
1
DATA
1
DATA
1
DATA
1
DATA
0
DATA
OFF HOOK
FRAME

FIG. 13A

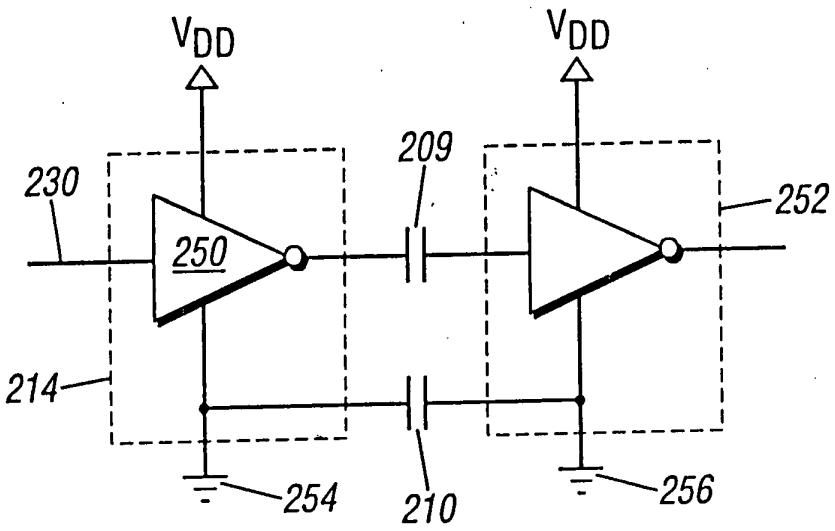


FIG. 13B

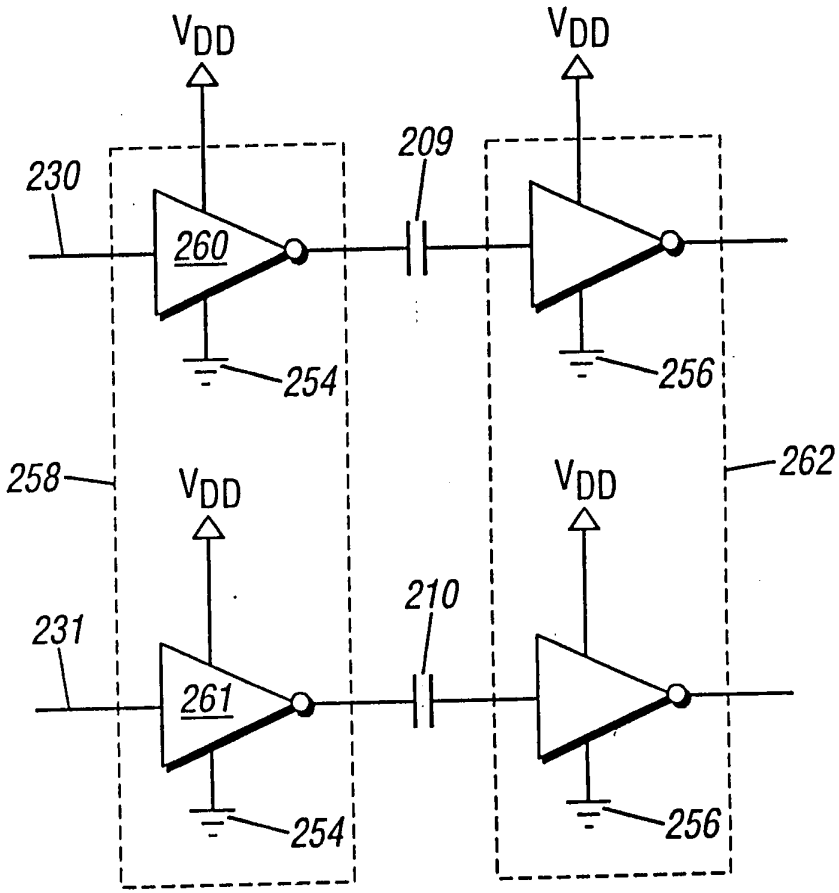


FIG. 14

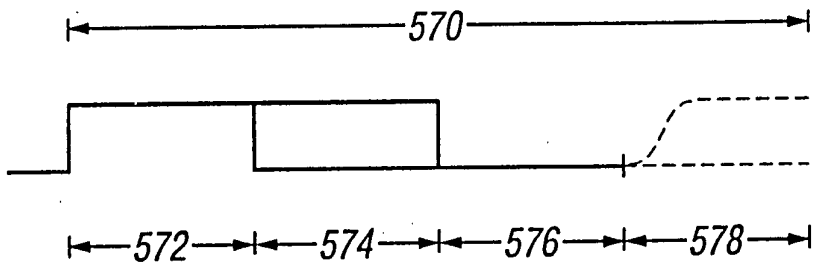

570
572
574
576
578

FIG. 15

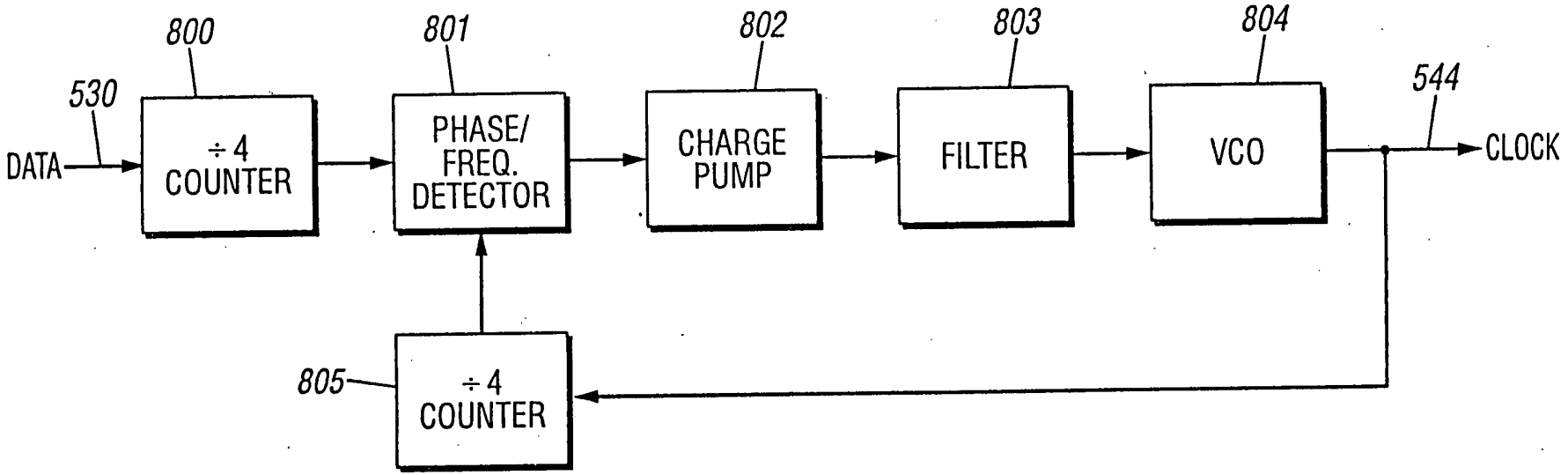

800
801
802
803
804
530
544
DATA
÷4 COUNTER
PHASE/ FREQ. DETECTOR
CHARGE PUMP
FILTER
VCO
CLOCK
805
÷4 COUNTER

FIG. 16

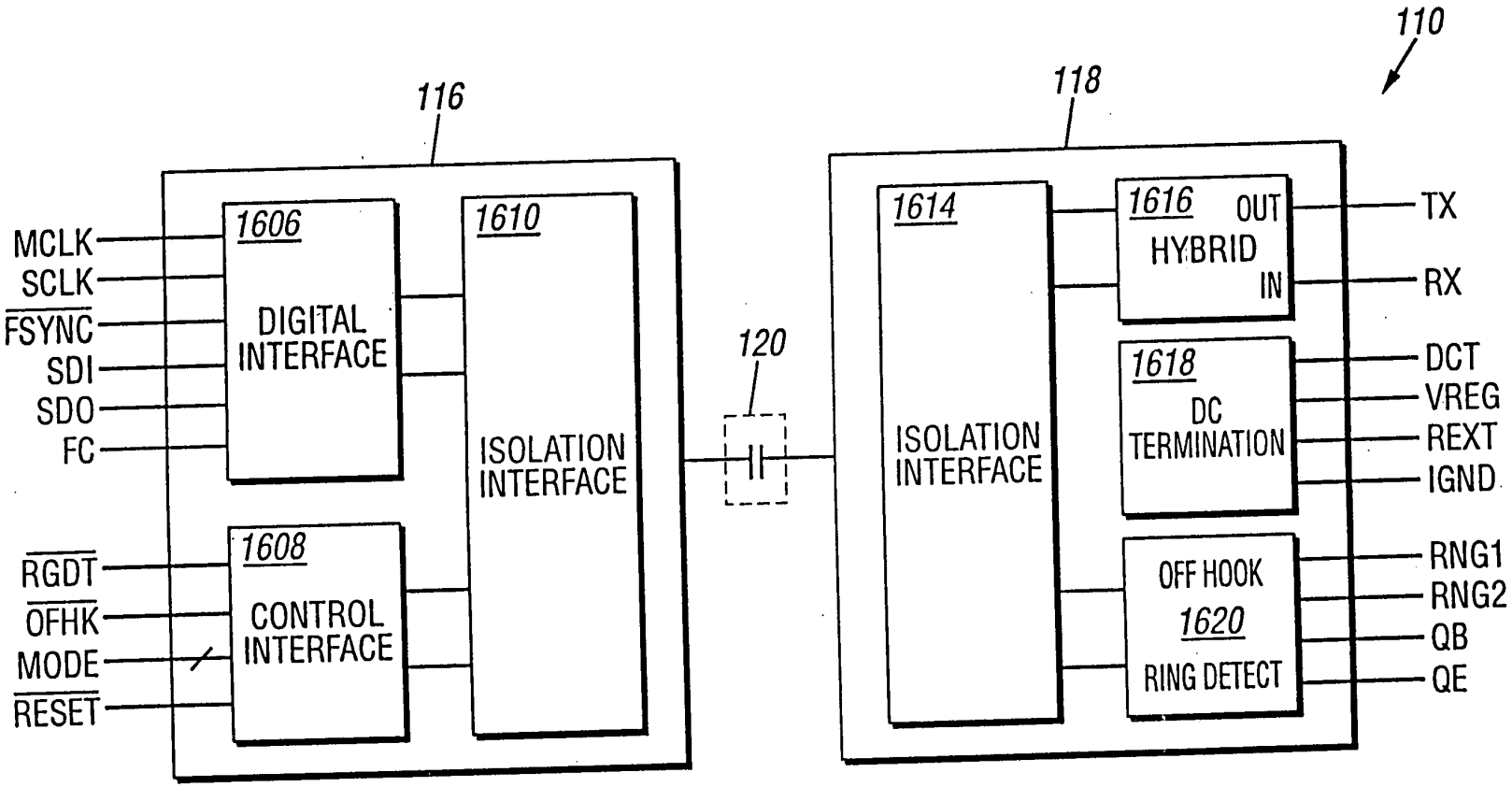

110
116
118
MCLK
SCLK
FSYNC
SDI
SDO
FC
1606
DIGITAL INTERFACE
1610
ISOLATION INTERFACE
120
RGDT
OFHK
MODE
RESET
1608
CONTROL INTERFACE
1614
ISOLATION INTERFACE
1616
HYBRID
OUT
IN
TX
RX
1618
DC TERMINATION
DCT
VREG
REXT
IGND
OFF HOOK
1620
RING DETECT
RNG1
RNG2
QB
QE

FIG. 17

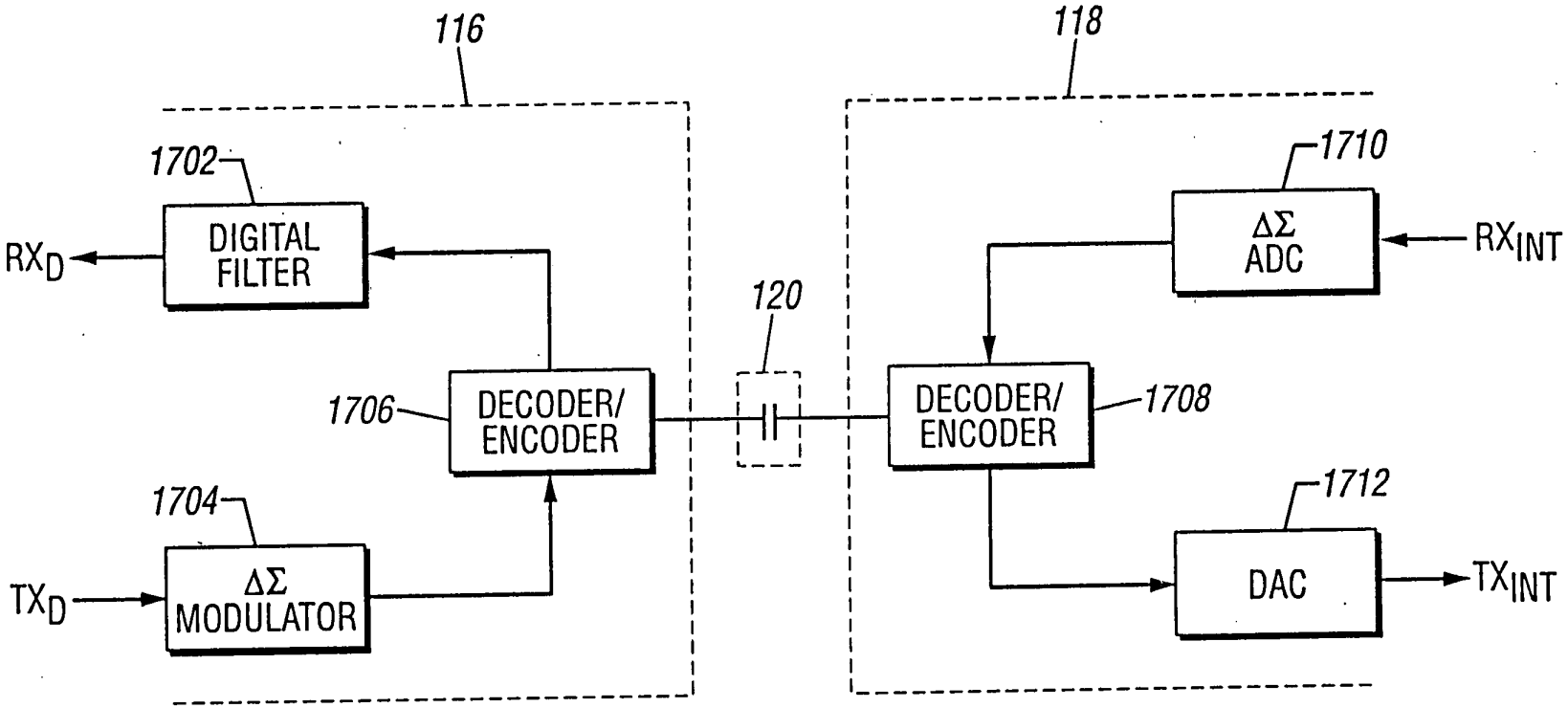

116
118
1702
DIGITAL FILTER
RX_D
1710
ΔΣ ADC
RX_{INT}
120
1706
DECODER/ ENCODER
DECODER/ ENCODER
1708
1704
ΔΣ MODULATOR
TX_D
1712
DAC
TX_{INT}

FIG. 18

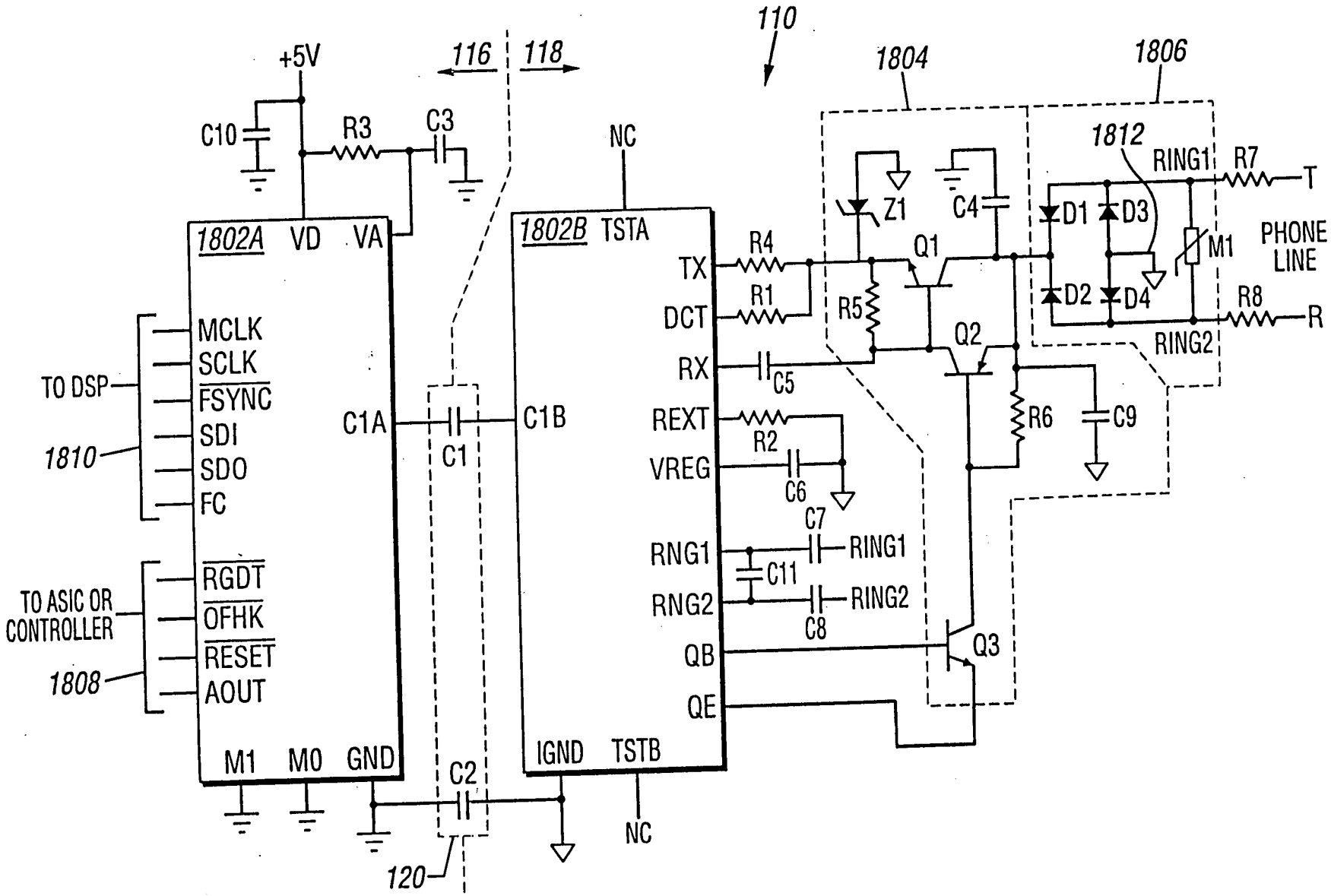

110
116
118
+5V
C10
R3
C3
NC
1804
1806
1812
1802A
VD
VA
1802B
TSTA
Z1
C4
RING1
R7
T
D1
D3
M1
PHONE LINE
R4
Q1
TX
R1
DCT
R5
D2
D4
R8
R
RING2
Q2
RX
C5
TO DSP
MCLK
SCLK
FSYNC
SDI
SDO
FC
1810
C1A
C1
C1B
REXT
R2
R6
C9
VREG
C6
C7
RNG1
RING1
C11
RNG2
RING2
C8
Q3
TO ASIC OR CONTROLLER
RGDT
OFHK
RESET
AOUT
1808
QB
QE
M1
M0
GND
C2
IGND
TSTB
NC
120

FIG 19

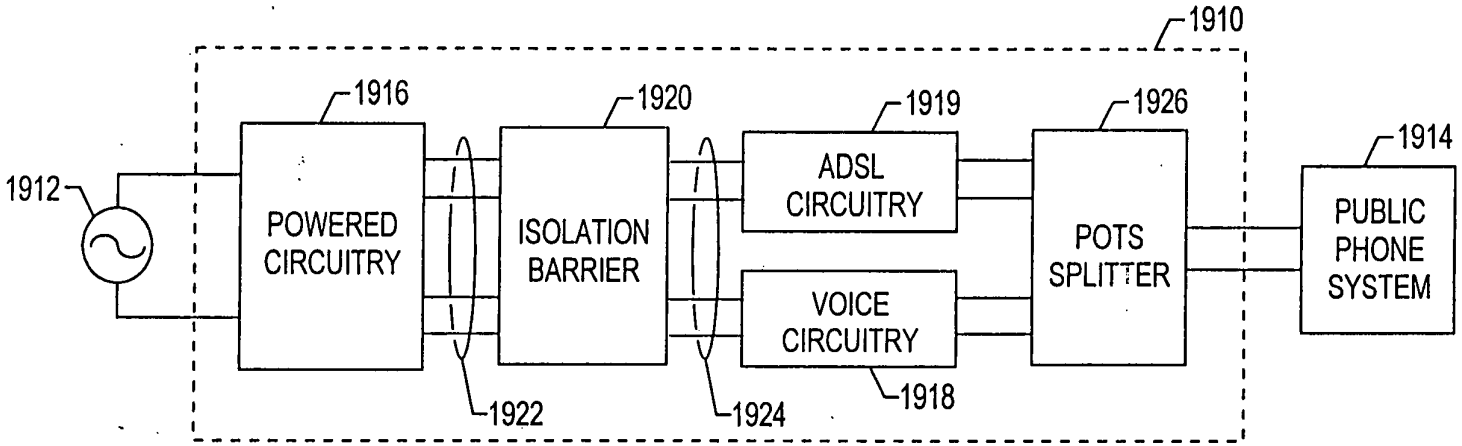
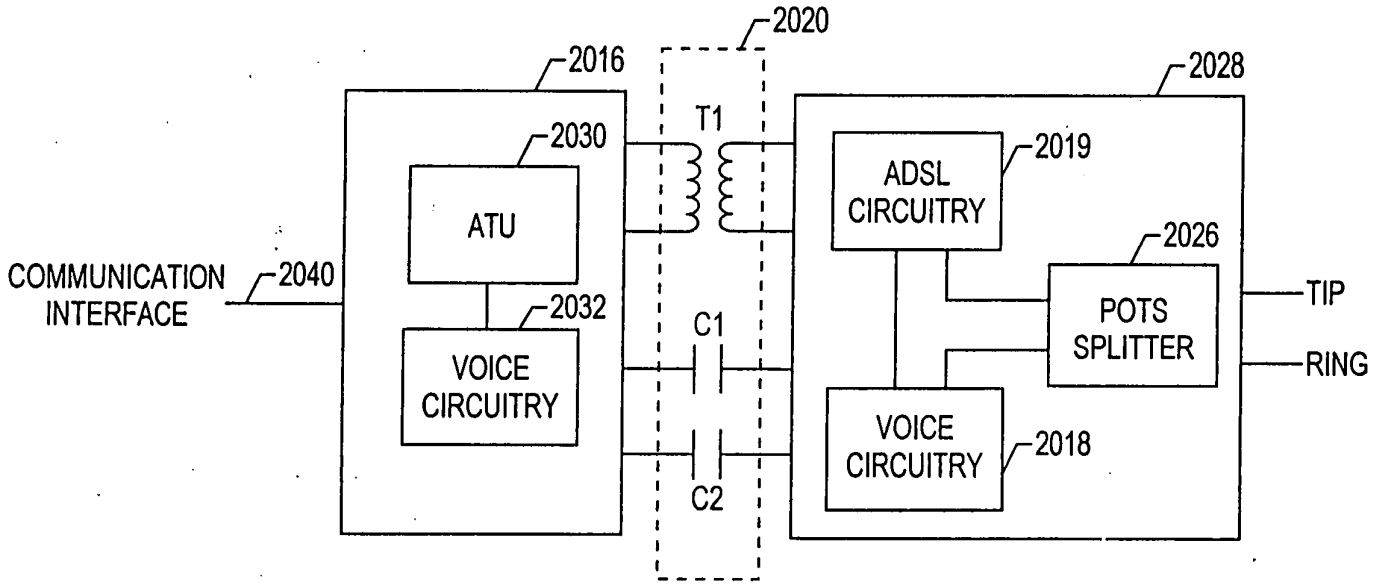

1910
1916
1920
1919
1926
1914
1912
POWERED CIRCUITRY
ISOLATION BARRIER
ADSL CIRCUITRY
VOICE CIRCUITRY
POTS SPLITTER
PUBLIC PHONE SYSTEM
1922
1924
1918

FIG20


2020
2016
2028
T1
2030
ATU
2019
ADSL CIRCUITRY
2026
COMMUNICATION INTERFACE
2040
2032
POTS SPLITTER
TIP
C1
VOICE CIRCUITRY
RING
VOICE CIRCUITRY
2018
C2